AMENDMENTS TO THE CLAIMS

1. (Currently amended) A system for device verification, wherein the system comprises

a profile generation module configured to provide a pattern profile that represents a sequence of input signal vectors with an associated sequence of output signal vectors (hereafter a "test pattern"), wherein the pattern profile includes a human-intelligible description of aspects of the test pattern, wherein the aspects are specified by a profile mode;

a coverage measurement module configured to process the pattern profile to produce analysis results indicative of coverage provided by the test pattern, wherein the profile generation module is further configured to process the analysis results to provide an improved pattern profile; and

a pattern generation module configured to receive the improved pattern profile and to convert the improved pattern profile into a test pattern for verifying device performance.

2. (Original) The system of claim 1, wherein the coverage measurement module is configured to determine coverage of the test pattern by ascertaining if node faults are detectable, wherein node faults are detectable if running the test pattern on a device would indicate a failure.

3. (Original) The system of claim 1, wherein the coverage measurement module ascertains if node faults are detectable for those nodes in a first category, and wherein the coverage measurement module ignores those nodes in a second category.

4. (Original) The system of claim 1, further comprising:

a test pattern profiling module configured to convert an existing test pattern into a pattern profile as specified by a profile mode.

5. (Original) The system of claim 1, further comprising:

a pattern checking module configured to process the pattern profile to produce analysis results indicative of whether the test pattern complies with a specified rule.

6. (Original) The system of claim 1, wherein the pattern generation module is coupled to run the test pattern on a device-under-test that implements at least a portion of a device design.

7. (Original) The system of claim 6, wherein the device design has a set of interesting input signals and a set of customary input signals, wherein the profile includes a human-intelligible representation of the set of interesting input signals, and wherein the profile does not include any representation of the set of customary input signals.

8. (Original) The system of claim 6, wherein the device design includes functional modules each having module input signals and module output signals.

9. (Original) The system of claim 8, wherein the profile includes a human-intelligible representation of a test pattern for one of the functional modules.

10. (Original) The system of claim 1, wherein the profile generation module is configurable to generate sequential permutations of values to specify pattern profiles.

11. (Currently amended) A system for verifying device designs that include functional modules, wherein the system comprises:

a profile generation means for providing a pattern profile that represents a sequence of input signal vectors with an associated sequence of output signal vectors (hereafter a "test pattern"), wherein the pattern profile includes an intelligible description of aspects of the test pattern, wherein the aspects are specified by a profile mode;

a coverage measurement means for analyzing the pattern profile to produce analysis results indicative of coverage provided by the test pattern, wherein the profile generation means is further configured to process the analysis results to provide an improved pattern profile; and

a pattern generation means for converting the improved pattern profile into a test pattern.

12. (Original) The system of claim 11, wherein the coverage measurement means is configured to determine coverage of the test pattern by ascertaining if node faults are detectable.

13. (Original) The system of claim 11, further comprising:

a test pattern profiling means for converting an existing test pattern into a pattern profile.

14. (Original) The system of claim 11, wherein the pattern generation means is coupled to run the test pattern on a device simulation means that implements at least a portion of a device design.

15. (Original) The system of claim 14, wherein the device design has a first set of input signals and a second distinct set of input signals, wherein the profile includes an intelligible representation of the first set of input signals, and wherein the profile does not include any representation of the second set of input signals.

16. (Original) The system of claim 14, wherein the device design includes functional modules each having module input signals and module output signals, and wherein the profile includes an intelligible representation of a test pattern for one of the functional modules.

17. (Currently amended) A method for verifying a device design using a sequence of input signal vectors with an associated sequence of output signal vectors (hereafter a "test pattern"), wherein the method comprises:

analyzing a test pattern profile to determine coverage of a test pattern;

generating a second profile for an improved test pattern that provides better coverage;

converting the second profile into the improved test pattern; and

running the improved test pattern on a simulated device.

18. (Original) The method of claim 17, wherein the test pattern profile includes an intelligible representation of aspects of the test pattern, and wherein the aspects are specified by a profile mode.

19. (Original) The method of claim 18, wherein one aspect specified by the profile mode is a subset of input signals that represent instructions.

20. (Original) The method of claim 18, wherein one aspect specified by the profile mode is a set of input signals for a functional sub-module of the device design.